ECE 303 Final Exam Cheat Sheet

To reduce delay in a logic cell

- **Decrease load:** use smaller transistors and shorter wires.
- **Increase drive strength:** widen transistors, but note this increases input load; keep small unless high drive is needed.

Setup Time Constraint

$$t_{pdmax} + t_{setup} + t_{pcq} < T_c \tag{1}$$

- t_{pdmax}: Maximum propagation delay through combinational logic

Hold Time Constraint

$$t_{pdmin} + t_{pcq} \geq t_{hold} \tag{2}$$

- t_{pdmin}: Minimum propagation delay through combinational logic

Sequential Logic

- D Flip-Flop (DFF): edge-triggered memory element
- Latches: level-triggered memory element
- Metastability: undefined state due to timing violations
- Ripple counter: asynchronous, slow
- Synchronous counter: all FFs share clock, preferred
- Shift register: shifts data left/right each cycle
- Moore machine: output depends on current state
- Mealy machine: output depends on state + input

FPGA and Programmable Logic

- PLA: programmable AND and OR planes
- PAL: programmable AND, fixed OR
- FPGA: field-programmable, uses LUTs, FFs, routing
- LUT (Look-Up Table): logic function via memory
- CLB (Configurable Logic Block): unit with LUTs + FFs

EDA Tools and Concepts

- RTL: Register Transfer Level, high-level design
- Synthesis: RTL $\rightarrow$ gate-level (Genus)
- Simulation: functional behavior check (Xcelium)
- Timing constraints: `.sdc` files define setup/load
- `.lib`, `.lef` files: standard cell definitions

Clock Tree

- **Clock skew**: Difference in clock arrival times at different flip-flops.
  - Must be included in timing analysis.
  - A primary source of setup/hold violations.
- **Clock jitter**: Random variation in clock edge timing due to noise or power fluctuations.
- **Clock power**: Clock distribution can consume 15–40% of total chip power.
- **Clock margining**: Total clock cycle includes logic delay, clock skew, and variation margins; all must fit within the clock period.